Silicon carbide photoconductive switch for high-power, linear-mode operations through sub-band-gap triggering

K. S. Kelkar, a) N. E. Islam, C. M. Fessler, and W. C. Nunnally Department of Electrical and Computer Engineering, University of Missouri, Columbia, Missouri 65211

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The analysis of a 6H silicon carbide (SiC) photoconductive switch, designed and packaged for high-power, linear-mode operations, is presented. The switch, fabricated from semi-insulating compensated SiC, is triggered by an optical source with photon energy less than the band-gap energy. Simulation models incorporating the effects of vanadium trap and nitrogen dopant in the compensation material show I-V characteristics that agree with measured values. The photoconductive switch has improved rise-time characteristics as compared to a gallium arsenide (GaAs) switch. The analysis also shows that improved performance at high power is possible through passivation using high-permittivity dielectric near the contact-semiconductor interface and by placing a p^+ layer next to the cathode. © 2005 American Institute of Physics.

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I. INTRODUCTION

In pulsed power systems, the power conditioning system performs such basic functions as storage, scaling, and switching. The performance of the switches used in generating the output pulse influences the volume and energy density of the system. The fundamental limitations on the system volume are determined by the maximum energy density of the dielectrics used for energy storage and the compactness of the switches employed in pulse shaping and scaling functions. A short-pulse-power delivery system, for example, can utilize a photoconductive semiconductor switch (PCSS) as the switching element. When used in a stacked Blumlein line (SBL) configuration, a one-to-one correlation must exist between the closing jitter and the rise time of the photoconductive switch.

Both Si and GaAs have been used as PCSS material for high-power applications. Because of its superior electrical characteristics, GaAs is preferred over Si in most pulse-power generation circuitry. However, when operated at a high repetition rate at sustained high power, GaAs switches are limited by poor thermal conductivity and are susceptible to failure either through premature breakdown or burnout. When photoconductive switches are operated in the nonlinear mode, filamentary conduction and charge trapping result in contact and bulk material damages. Linear-mode operation, in which the current is distributed over a large cross section, is an alternate approach to switch design for high-power operation. In any high-power system, the PCSS material must meet the rigorous requirements of high fields, large current densities, and high thermal conductivity.

High-resistivity SiC with high breakdown field, large thermal conductivity and stability, a wide energy band gap, mechanical robustness, and a reasonable electron saturation velocity is a potentially better PCSS material than GaAs. SiC can be operated in the linear photoconductive mode and under extreme operating conditions and yet delivers high power. ^{9,10} The picosecond jitter associated with linear photoconductive switches is also an advantage. ¹ Thus this study was conducted to study and characterize high-resistivity SiC as a PCSS material for high-power applications.

This research was conducted in collaboration with the Lawrence Livermore National Laboratory (LLNL), where most of the switches are being fabricated. We specifically look into the material characteristics, carrier transport mechanisms, and possible design changes in the PCSS to optimize its performance. In addition, we have investigated the compensation mechanisms that result in high-resistivity semi-insulating 6*H*-SiC. This discussion is followed by a brief description of the PCSS, experimental setup, and *I-V* measurements. We detail the simulation setup and analysis in Secs. III and IV, respectively, and conclude in Sec. V.

II. COMPENSATION MECHANISMS IN 6H-SIC

The evaluated and analyzed PCSS's are fabricated from 6H-SiC semi-insulating materials that are grown through the compensation process. Compensation results when the ionized donor and acceptor densities effectively cancel each other such that the net density of free carriers in the semiconductor is very small. Two types of compensation structures have been investigated: (1) deep trap donor levels compensated by shallow level dopants, termed as the DDSA structure, and (2) shallow donor dopants compensated by deep acceptor levels, termed as the SDDA structure. At room temperature the shallow dopant level is completely ionized and the deep traps are partially ionized, which make the material semi-insulating. In 6H-SiC the two deep trap levels, both acceptors and donors are formed by vanadium. The V^{3+}/V^{4+} acceptor trap level is present at 0.74 eV from the conduction band¹¹ and a deep donor trap level (V^{4+}/V^{5+}) is present at 1.6 eV, close to the middle of the band gap. 12 Deep levels other than vanadium, ¹³ because of their low concentration, are usually not used in the analysis. The shallow dopant that is compensated is nitrogen or boron. Nitrogen is

a)Electronic mail: kskpnb@mizzou.edu

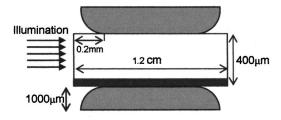




FIG. 1. Switch geometry.

absorbed at porous graphite parts and boron is inherently present in crucible material. Thus, the material is classified as shallow donor-deep acceptor (SDDA, V^{3+}/V^{4+} compensated with nitrogen) or deep donor shallow acceptor (DDSA, V^{4+}/V^{5+} compensated with boron) type.

Nitrogen in the SDDA-type 6H-SiC is located at E_C -0.081, $E_{\rm C}$ -0.138, and $E_{\rm C}$ -0.142 eV from the conduction band and is completely ionized at room temperature. 16 The acceptor level is a hole trap. It is neutral when empty and negatively charged when filled. Thus an acceptorlike trap is negatively charged and may emit an electron. This explains the location of the acceptorlike trap from the conduction band. In the DDSA SiC, vanadium is compensated by boron at $E_V + 0.3$ from the valence band. 12 The donor level is an electron trap. It is positive when empty and neutral when filled. The PCSS used in this analysis is the SDDA type and the device configuration is shown in Fig. 1. The length and the width of the device are $1.2 \times 1.2 \text{ cm}^2$ and is approximately 350-400 µm in depth. The radius of contact curvature is 0.2 cm. The contact leaves the 6H-SiC slab around 0.4 cm from the center of the switch. The nickel silicide contacts have a resistivity of about $1 \times 10^{-5} \Omega$ cm. ¹⁷ The actual contacts are made up of NiSi2/Ti/Pt/Au/Cu layers with thicknesses of 200/200/100/100/500 nm, respectively. The SiC component of the PCSS in Fig. 1 can be seen as the small rectangular disk in the middle of the contacts. A high-voltage power supply is connected in series with a 10 M Ω resistance, a switch under test, and a picoammeter. The 10 M Ω resistor is used to limit the current through the switch in case of breakdown. Kiethley 6485 picoammeter has a least count of 1 FA. A Tektronix P6015A high-voltage probe with an input resistance of 100 M Ω is used to measure the voltage across the switch and the measurement is read out on a Tektronix DTS 7404 digital phosphor oscilloscope. Following initial dc I-V tests and material characterization, the devices are expected to be tested for high-power pulse mode.

III. SIMULATION SETUP: MATERIAL AND MODEL PARAMETERS

High-resistivity compensated semiconductors with high trap densities have conduction characteristics that are similar to "lifetime" materials as opposed to intrinsic "relaxation" materials.¹⁸ Simulations therefore involve the solution of the basic semiconductor continuity and Poisson's equations shown below. The generation and recombination terms, however, are defined through traps and dopant parameters that are inherent to the material,

$$\frac{\partial n}{\partial t} = \frac{1}{q} \operatorname{div} J_n + G_n - R_n, \tag{1}$$

$$\frac{\partial p}{\partial t} = \frac{1}{q} \operatorname{div} J_p + G_p - R_p, \tag{2}$$

$$J_n = qn\mu_n E_n + qD_n \nabla n, \tag{3}$$

$$J_p = qp\mu_p E_p - qD_p \nabla p, \tag{4}$$

$$\frac{dE}{dx} = \frac{q}{\epsilon} (p - n + N_t^{\dagger}). \tag{5}$$

Here q is the magnitude of the charge on an electron $(1.6 \times 10^{-19} C)$, n and p are the electron and hole concentrations, respectively, J_n and J_p are the electron and hole current densities, G_n and G_p are the generation rates of electron and holes, R_n and R_p are the recombination rates for electrons and holes, μ_p and μ_n are the hole and electron mobilities, and D_n and D_p are the electron and hole diffusivities, respectively. Models emphasizing physical parameters such as trap level, its density of states, energy states and their cross sections along with Shockley-Read-Hall (SRH) and Auger recombination models, concentration- and field-dependent mobility models, and impact ionization are also considered and solved analytically. These parameters influence carrier lifetimes, pulse decay, diffusion, and the Debye length. In fact, the trap concentration level and its influence in the Debye length have a major influence in making a high-resistivity compensated material behave like a lifetime semiconductor, as detailed in Ref. 18.

For compensated materials, additional equations and models are required to compute the densities of the trapped carriers that relate to the generation and recombination terms in Eqs. (1) and (2) presented above. These models use electron- and hole-capture cross sections, density of trap centers, degeneracy of the electron and hole trap centers, and the Fermi-level position for computation. The models thus incorporate the physics associated with charge exchange with the conduction and valance bands, changes in space-charge density, and recombination statistics in the solution. The densities of trapped carriers at a trap center for respective carrier types are given by Eqs. (6) and (7), ¹⁹

$$n_t = \sum_{\alpha=1}^k n_t^{\alpha},\tag{6}$$

$$p_t = \sum_{\beta=1}^m p_t^{\beta},\tag{7}$$

where k=number of acceptorlike traps and m=number of donorlike traps. n_t^{α} and p_t^{β} are defined as

$$n_t^{\alpha} = N_{\text{ta}}^{\alpha} \frac{K_n^{\alpha} + G_p^{\alpha}}{G_p^{\alpha} + G_n^{\alpha} + K_p^{\alpha} + K_n^{\alpha}},$$
 (8)

$$p_t^{\beta} = N_{\text{td}}^{\beta} \frac{K_p^{\beta} + G_n^{\beta}}{G_p^{\beta} + G_n^{\beta} + K_p^{\beta} K_n^{\beta}},\tag{9}$$

$$K_p = p\sigma_p V_p, \tag{10}$$

$$K_n = n\sigma_n V_n, \tag{11}$$

$$G_p = \frac{1}{\gamma} \sigma_p V_p n_i \exp\left(\frac{\varepsilon_i - \varepsilon t}{kT}\right),\tag{12}$$

$$G_n = \frac{1}{\gamma} \sigma_n V_n n_i \exp\left(-\frac{\varepsilon_i - \varepsilon t}{kT}\right),\tag{13}$$

where ε_i =intrinsic Fermi-level position, γ =degeneracy factor of the trap level, V_n and V_p =thermal velocities, σ_n and σ_p =carrier capture cross sections, $N_{\rm ta}$ and $N_{\rm td}$ =density of trap centers, and ε_t =energy level of the discrete trap state. Subscripts n and p are used for electrons and holes, respectively.

To account for the effects of trapped charge, an additional charge term is assigned to the right-hand side of Poisson's Eq. (5). This charge term is equal to the difference in the densities of the trapped carriers multiplied by the electronic charge. The recombination models in Eqs. (1) and (2) also need modification with a correction term that accounts for trapping and detrapping effects. The transient solution needs to account for trap density changes over time through the solution of additional trap rate equations.

IV. SIMULATION RESULTS AND DISCUSSIONS

In the simulation process, a reasonable match of the measured and simulated I-V characteristics ensures that the right material has been used in the analysis. Measured material parameters are therefore very essential as simulation inputs. However, it is not always possible to get all the necessary material parameters. It is mainly because some parameters vary from one batch to another and also between vendors (who usually do not volunteer information on trap levels, cross sections, etc.). Some of the material data used in the simulations were provided by the vendor, ²⁰ while the trap energy level and cross sections were taken from Ref. 11. No information on compensation ratio (defined later) was available and its value was therefore adjusted to match the experimental I-V. The switch resistance prior to the testing was around 65 M Ω . Considering an area of 1.44 cm² and 0.04 cm switch length, the calculated resistivity value (~2 $\times 10^9 \ \Omega$ cm) is consistent with the vendor information.²⁰

The PCSS model simulated with SILVACOTM codes is shown in Fig. 1. A two-dimensional (2D) device with reduced number of mesh points (\sim 8000) was used for simulations rather than a three-dimensional (3D) setup with 96 000 mesh points. The 2D setup reduces the simulation time considerably without affecting the overall accuracy of the results sought in the analysis. A 200- μ m-thick nickel silicide, which is in intimate contact with SiC, was used as the contact ma-

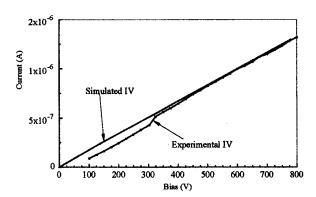


FIG. 2. Experimental and simulated I-V characteristics.

terial for simulations. Other contact materials that are deposited on top of the silicide layer are not expected to affect the injection mechanism in the device and hence are neglected in the simulation. Figure 2 shows the measured and simulated *I-V* for the device. The simulated *I-V* was obtained as follows.

The concentration of nitrogen dopant, as supplied by the vendor, was found to be $(2-7) \times 10^{15}/\mathrm{cm}^3$. Vanadium trap concentration was increased in steps to get a compensation ratio that matches with the measured I-V (Fig. 3). A good match was possible for vanadium concentration of $2 \times 10^6/\mathrm{cm}^3$, which gives a compensation ratio of 10. Since there are two trap levels present in the semi-insulating 6H-SiC, is simulations were also carried out with two traps and also with each individual trap present in the material. The best correlation with the measured I-V characteristics was possible with one single trap level at E_C –0.74 eV (2.28 eV). This level is assumed to be the dominant trap level and is used in the subsequent simulations. The dominance of the single trap level is due to its proximity to the Fermi level as discussed below.

In trap-dominated materials, the trap energy level, its density, and capture cross sections also affect the material parameters and its charge conduction characteristic. Affected material parameters include the location of the Fermi level (E_F) which determines whether a trap level (E_t) is shallow or deep. For a shallow trap, E_F lies below the trap level and for a deep trap, E_F lies above E_t . The location of the Fermi level in the bulk of the semi-insulating region is determined from space-charge neutrality requirements. Since the position of

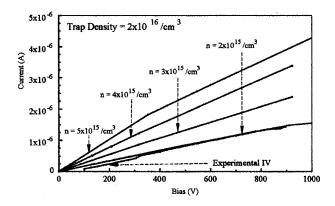


FIG. 3. Effect of compensation ratio on the slope of the I-V characteristics.

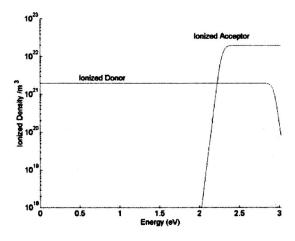


FIG. 4. Shockley plot.

the Fermi level can be influenced by any of the impurity levels, as well as the free-carrier densities, the conditions for the space-charge neutrality for a compensated material become more difficult to isolate. For compensated materials that include traps and donor/acceptor levels, the Fermi level also changes and influences the conduction process. For the SDDA material under consideration, the Fermi-level position can be set as shown in Eq. (14),²¹

$$E_{F,st} = E_{da} - K_B T \ln g_{da} - k_B T \ln(m-1), \tag{14}$$

where $m = (N_{da}/N_{sd}) N_{da}$ = density of the deep acceptor level (cm⁻³), $N_{\rm sd}$ =density of the shallow donor level (cm⁻³), g_{da} =occupancy of the deep acceptor level, E_F =Fermi energy level (eV), E_{da} =deep acceptor energy level (eV), k_B =Boltzmann's constant, and T=temperature (K). This is in contrast to the Fermi-level equation for intrinsic material that does not depend on the compensation ratio m. A typical Shockley plot, prior to laser application in the active region of the PCSS, is shown in Fig. 4 for a compensation ratio of 10. At the onset of the conduction process, the Fermi level tends to move up/down as more and more trap levels are filled and the compensation ratio changes. On the other hand, the free-carrier densities have little or no impact on the position of the Fermi level, which is a characteristic and desirable feature of the semi-insulating material. The plot shows a Fermi level at 0.833 eV from the conduction band (2.187 eV from the valence band). Since the intrinsic energy level is located at 1.511 eV from the valence band, the material is n

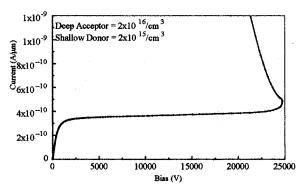


FIG. 5. Simulated *I-V* till breakdown.



FIG. 6. Lateral mismatch between the contact layers causing damage to the SiC.

type. Such traps sites, also classified as acceptors (0/-), will influence the conduction process. The Shockley plots are consistent with the plots based on similar equations for compensated SDDA GaAs.²¹ Here, as the compensation ratio increases, the Fermi level moves down and is in agreement with the observations of Bickermann *et al.*²²

With the device material type verified for simulations, breakdown analysis and high-power design changes were also studied. The initial dc tests of the switch at LLNL indicated early breakdown around 15 kV. Figure 5 shows the simulated *I-V* characteristics at high applied voltages. The electric field and trap occupancy were closely observed as the bias increased which shows a breakdown at 24 kV. The experimental breakdown at 15 kV has been attributed to a lateral mismatch in the contact layer (Fig. 6). While trap occupancy was limited to the bulk region, high field regions are observed close to the anode increasing the impact ionization rate as shown in Fig. 7, which ultimately leads to breakdown. A comparative study shows that the SiC PCSS fares better in high-blocking-voltage operation.

A GaAs switch studied earlier with a distance of 0.25 cm between the contacts has a simulated breakdown voltage of 34 kV.⁵ In the case of the SiC PCSS an improvement in the breakdown field is obvious, since the distance between the contacts is 0.04 cm with a breakdown voltage of 24 kV. It is expected that with pulse charging, rather than dc charging,

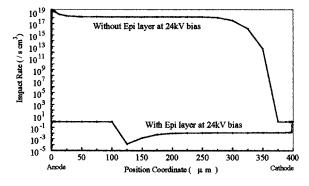


FIG. 7. Impact ionization profile with and without the epilayer at the cathode at 24 kV.

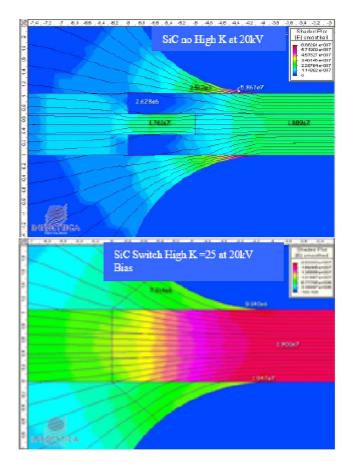


FIG. 8. (Color online) Effect of high k on the electric field at the surface.

the measured breakdown value will improve further. A simulation of DDSA GaAs with the SiC contact distance results in a breakdown voltage of 5 kV.

Like Si PCSS, improvement in the premature breakdown is possible with proper surface passivation and beveling the device edges.²³ We have also investigated the use of highpermittivity (high-k) passivation material for improving the surface dielectric strength and a possible improvement in early breakdown. The effect of high-k material and its effect on the electric fields in the separation region between the semiconductor and the contact are simulated and are shown in Fig. 8 for a 20 kV bias. By having passivation layers with increasing permittivity values, it was determined that the electric field generated in the gaps is reduced by an order of magnitude with a permittivity of 25 as compared with vacuum. This is because the electrostatic boundary conditions between dielectric interfaces dictate that a reduction in electric field is possible if the permittivity is high and the charge density at the interface is low. A good bond at the interface reduces the charge density and so does the use of a high-permittivity material. It is expected that such a configuration will enable device operation at higher bias without damage to the contacts as well as reduce arcing between the electrodes, thus preventing premature breakdown.

The use of n^+ layer to inhibit the electron injection until higher bias voltages, which improves the hold off voltage of the device, has been previously shown.⁵ For the PCSS under study a p^+ -Si (SDDA) 6H-SiC junction has similar effect.

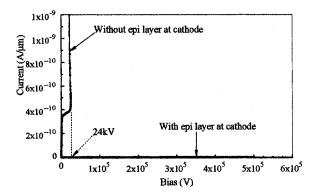


FIG. 9. Improvement in the hold off voltage due to the p^+ layer at the cathode.

This is because the device material is n type and thus a p^+ -n junction is formed. The field lines for this junction are opposite to the externally applied electric field which results in carrier injection at a higher bias, which also limits the effect of impact ionization. An improvement in the breakdown characteristics can therefore occur.

A comparison of the device I-V with and without the p^+ layer at the cathode is shown in Fig. 9. Figure 7 (explained earlier) shows the impact rate at 24 kV with and without the epilayer at the cathode. As can be seen from the plot, the impact rate is restricted to very low values by the use of the epilayer. This structure results in a large improvement in the hold off voltage for 6H-SiC PCSS with a p^+ layer at the cathode over an earlier GaAs design (Ref. 5). The improved blocking voltage characteristic with the p^+ layer is shown in Fig. 10.

For DDSA GaAs the *EL2* level has an electron lifetime of 0.5 ns.²¹ For SDDA SiC the lifetime of the V³⁺/V⁴⁺ level is five times higher, as calculated from the capture cross section, density of states, and maximum thermal velocity. Hence for the same switch geometry, SDDA 6*H*-SiC will give better rise time since the trapping detrapping will be slower than GaAs, avoiding initial kinks in the pulse.⁵ In fact, for the University of Missouri-Columbia. (UMC) geometry, the distance between contacts is shorter for the SiC PCSS; the transit time between the electrodes is less, thus

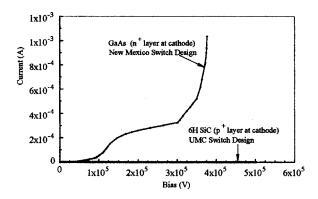


FIG. 10. Comparison of the UMC geometry *I-V* characteristics to the New Mexico switch design.

improving the rise time further. As a result, more energy can be transferred to the load in the SiC PCSS, as compared to GaAs.

V. CONCLUSION

Semi-insulating compensated SiC has been investigated as the working material in a linear, extrinsic photoconductive switch with a geometry. The geometry and package as well as the underlying physics have been analyzed for high-power operation in the linear mode. The dc I-V characteristics of PCSS were used to calibrate the simulations and the simulations were adjusted to determine the material composition. The matching of experimental and simulated I-V characteristics ensures proper material identification. Two types of compensation structures were investigated and the role of traps in the compensated material correlated with experimental results. A method of increasing the high field breakdown for better rise time and to avoid surface flashover was investigated using high-K dielectric as passivation material in the region where the electrodes separate from the bulk switch material. Reduction in electron injection was devised through modeling of the device physics that increases the blocking voltage of the material. Simulations show that an increase in breakdown performance is achieved by placing a p^+ layer next to the cathode. Simulations also show that the 6H-SiC has better rise-time characteristics as compared to an earlier GaAs PCSS.

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